A 13-bit universal column driver for various displays of OLED and LCD

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Abstract — A universal column driver is implemented in a 0.13-μm high-voltage CMOS process for not only TFT-LCD but also OLED applications. The proposed column driver employs 13-bit linear DAC to cover all gamma curves of display applications and address-based configuration for intra- panel interface protocol to support both TV and IT applications. Measured results demonstrate the average voltage of output channels (AVO) is under 1mv, which satisfies 1-LSB resolution at 18.5V of AVDD.

Keywords — *Digital-to-analog converter(DAC), display driver, liquid crystal display(LCD), organic light-emitting diode(OLED), voltage interpolation.*

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1 Introduction

Active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode (AMOLED) are widely used in flat panel display as the display unit of TVs, tablets, laptops, and desktop monitors. In both display systems, the column driver IC plays a key role of reconstruction analog signals by digital-to-analog conversion from digital input data. A column driver generally includes shift registers, input-registers, data latches, level shifters, DACs and output buffers. Among those, the architecture of DACs are different as applications since the required analog voltage for same input digital data is different.

In AMLCD display systems, the liquid crystal material is used to control transmittance of light from back light unit. Transmittance of a liquid crystal exhibits a non-linear relationship to the applied voltage. To obtain a linear luminance output from an LCD in response to a digital input, the output of DAC is usually designed to be the inversion of the liquid crystal transmittance-voltage characteristic. That is, intervals between increments in voltage must be adjusted to compensate for non-linearity of the characteristic curve. This adjustment is called gamma correction. In order to implement a non-linear DAC, certain gamma voltages are applied a resistor string which is made up of resistors of unequal values, selected to produce required curve. Additionally, a non-linear DAC should supply both positive and negative polarity voltages between the LC cells with respect to a common backside electrode for a digital sub-pixel code to improve the lifetime of the LC material.[1,2] Hence, the column driver for LCD comprises two non-linear resistor strings for positive and negative polarity.

AMOLEDs are a self-emitting display, which does not need an external light source. There are two kinds of method to produce full color in AMOLEDs. Separate OLED materials for red, green and blue can be used to produce full colors. The separate OLED display is suitable for mobile application such as smart phones and tablets, because it is difficult to gain uniformity in large size panel. Separate color filters and white OLED can be used to produce full colors. This method is similar to LCD system in using color filter to separate red, green and blue colors so that white OLED system is suitable for large display systems such as TVs. Those organic materials do not require the inversion method to improve life time of the materials. But the gamma characteristics of three colors do not match, so the gamma correction needs to be separately provided for each color.[3,4] Otherwise, the color shift of the display might come up, because the transmittances of three colors are different even with same digital input data. Therefore, the column driver for OLED needs to realize separated DACs to support separate gamma corrections. Moreover, the data protocol between timing controller(TCON) and column drivers is various according to applications.[5,6] Because of this difference, column drivers have been developed for each application. To drive both displays with one column driver, two kinds of DAC for each gamma curve of LCD and OLED are needed as well two kinds of receiver. Therefore, these requirements cause a problem to increase chip size prohibitively.

In this paper, a 13-bit universal column driver IC is proposed to minimize increment of the chip size. The proposed column driver comprises a common 10-bit linear resistor string, 10-bit two voltages selectors, 3-bit 2 to 4 decoder and weighted 4-input interpolation amplifiers. The 13-bit linear DAC is implemented with the combination of 10-bit R-DAC and 3-bit interpolation amplifier. With 13-bit linear

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DAC and address based intra-panel interface protocol, the proposed column driver IC can drive not only LCDs but also OLEDs in all large display applications such as TVs, tablets, laptops and desktop monitors. The proposed column driver IC can be a good solution for hybrid display system using both LCD and OLED such as IOT products, future car display.

2 Proposed universal column driver

To avoid substantial growth in size of column driver die, a proposed universal column driver uses high resolution linear DACs to cover all gamma curves of LCD and OLED applications. These applications differ from not only gamma curve but also dynamic range. In order to generate all required DAC outputs of both LCD and OLED with one linear DAC, 1-LSB of the linear DAC should be smaller than required minimum 1-LSB of applications. Table 1 shows minimum 1-LSB requirement as applications. The required minimum 1-LSB in 10-bit OLED application is 3.41mV. As a result, a 13-bit resolution of the linear DAC is needed to have smaller 1-LSB than 3.41mv because 1- LSB of 13-bit linear DAC is 2.2mv at 18.5V of supply voltage. Therefore, a proposed universal column driver uses 13-bit linear DACs to cover all gamma curves of OLEDs and LCDs.

TABLE 1 — Minimum 1-LSB requirements as applications.

	Minimum 1-LSB	
Resolution	LCD	OLED
Non linear 8-bit	25mV	13.67mV
Non linear 10-bit	6.25mV	3.41mV

Figure 1 shows 10-bit non linear gamma curve corrections of LCD and OLED with 13-bit linear DAC outputs. Display applications using 10-bit non linear gamma transfer image data with 10-bit to TCON. TCON should change 10-bit to 13-bit data for 13-bit column driver so that the look up table is required for transforming 10-bit to 13-bit input data with same gamma voltage.

The uniform performance among the driver channels is one of the most important requirements for column driver ICs, because a column driver IC comprises hundreds of column driver channels. If inter channel uniformity is not guaranteed, fixed pattern noise tends to be detected from the display image. The resistor-string DAC(R-DAC) architecture has been generally utilized due to its uniform characteristic that stems from the commonly shared resistor-string for gamma reference generation.[7] However, the area of R-DAC and its related routing lines are prohibitively large for a high-resolution data converter. So, various combinations of R-DAC and interpolation have been proposed to achieve both high area-efficient design and high resolution

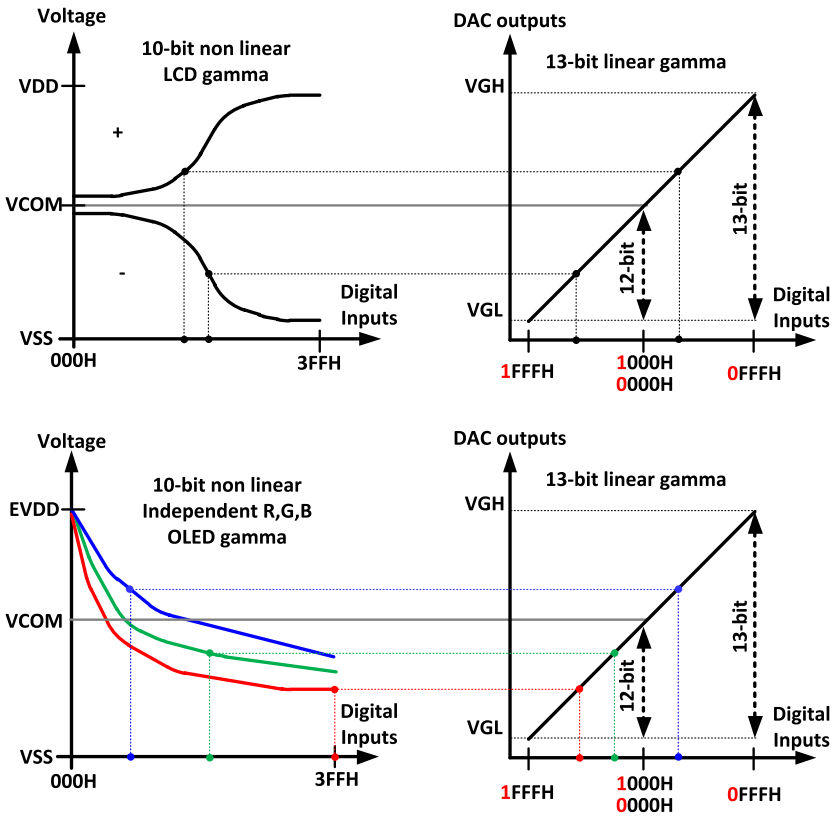

FIGURE 1 — 10-bit non linear gamma curve corrections of LCD and OLED with 13-bit linear DAC outputs.

performance.[8–13] As the number of interpolation bit increases, metal routings of decoder can be reduced. However, static power consumption of the interpolation amplifier will be increased and the speed of D/A conversion will be slowed down.

The architecture of a proposed 13-bit column driver IC is presented in Fig. 2. The proposed combination of R-DAC and interpolation is 10-bit for R-DAC and 3-bit for interpolation DAC. The 10-bit R-DAC consists of two voltages selectors and a common resistor string. The common resistor string produce 1024 voltage levels between VREFH and VREFL for all channel drivers. Based on the higher 10-bit signals (D3~D12), two voltages of VH and VL are selected from 1024 divided voltages and connected to a 3-bit interpolation amplifier. With the lower 3-bit signals(D0~D2), the 3-bit 2 to 4 decoder and 3-bit interpolation amplifier divides 8 voltage levels with same interval between VH and VL.

2.1 Gamma voltage generation

A proposed 13-bit column driver is consisted of hundreds of R-DACs. Those DACs share one common resister string so that inter channel uniformity is better than other architecture of DACs such as C-DAC. However, variation of resistors between column driver ICs cause display failure such as block dim. To prevent this display failure, additional voltages between VREFH and VREFL are required to minimize chip to chip variation of 1024 gamma voltages. Figure 3 (a) shows the architecture of digital gamma for producing additional voltages between VREFH and VREFL. This architecture is widely used in column driver because of low cost in display system. But drawback of the digital gamma architecture is the offset voltage of the gamma buffers. To reduce the offset voltage of the gamma buffers, the size of gamma buffers

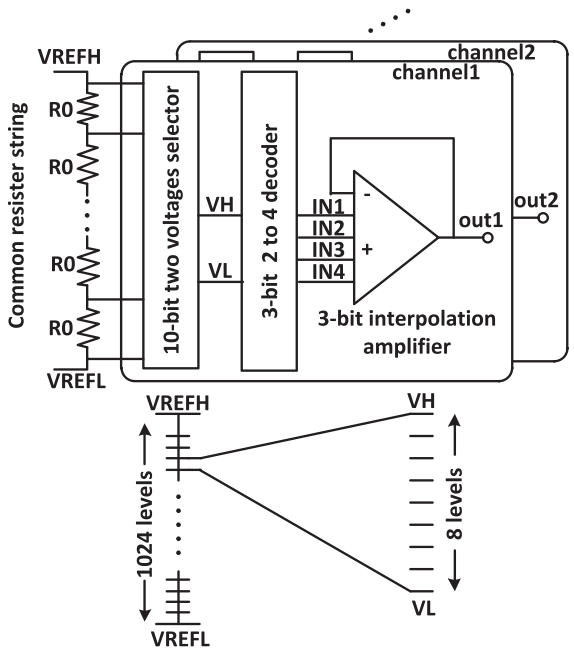

FIGURE 2 — The architecture of a proposed 13-bit column driver IC.

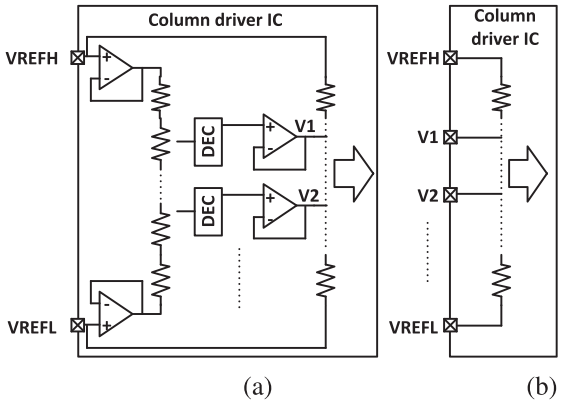

FIGURE 3 — The architecture of gamma voltage generation (a) digital gamma (b) external gamma.

should be increased. It cause chip size increase prohibitively because tens of gamma buffers are required. A proposed 13-bit column driver use external gamma voltage sources to remove aforementioned offset problems shown in Fig. 3 (b).

The number of gamma voltages between VREFH and VREFL determines not only chip to chip gamma voltage variations but also slew rate of output buffers. Large amount of current is instantaneously flow through the common resistor string on moment of transition because hundreds of input capacitors of amplifiers are connected to the common resistor string. This cause input delay so that slew rate is getting slow. The high resolution display applications require fast slew rate so that the input delay is critical. A proposed column driver uses 25 external gamma reference voltages to satisfy this high speed requirement.

2.2 10-bit two voltages selector

The 10-bit two voltages selector occupy most of die area because of two decoder paths for VH and VL and 1024 analog voltage paths. The conventional tree type 10-bit two voltages selector shown in Fig. 4. (a) causes not only chip size increase prohibitively but also input delay since 10-TRs are required on each decoder path. Figure 4 (b) shows proposed quaternary decoder for 10-bit two voltages selector. The proposed quaternary decoder reduces a half of TRs on each decoder path so that it can be implemented under die size limitation. Moreover, reducing the number of TRs on decoder path can reduce input delay, which is critical for high slew operation.[14] The proposed quaternary decoder demands data encoding with additional circuits. Table 2 shows example of 2-bit data encoding for quaternary decoder. Encoding circuits are implemented low voltage circuits so that size impact is lower than using conventional tree type decoder in 10-bit two voltage selector.

Symmetric gamma voltages with respect to VCOM are selected based on 9-bit (D3~D11). MSB 1-bit (D12) determines positive and negative with respect to VCOM. When D12 is high, positive gamma voltages are selected. When D12 is low, negative gamma voltage are selected. This 1-bit operates like a polarity control signal in LCD column driver.

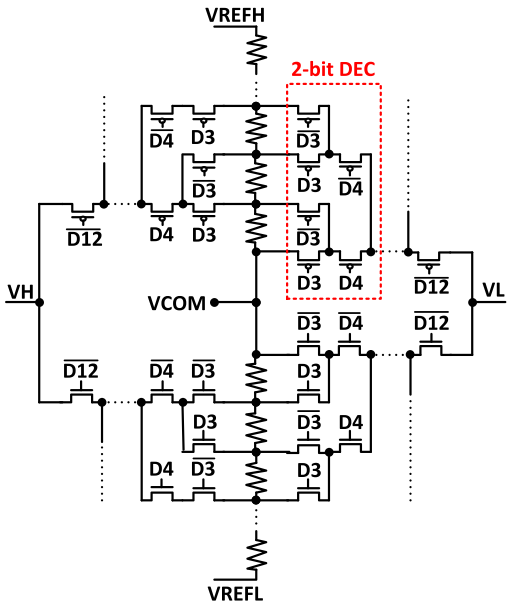

FIGURE 4 — 10-bit two voltages selector (a) conventional tree type decoder (b) proposed quaternary decoder.

TABLE 2 — 2-bit encoding for quaternary decoder.

D4	D3	DQ10	DQ11	DQ12	DQ13
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

2.3 3-bit interpolation amplifier

Figure 5 shows a simplified schematic of the proposed 3-bit interpolation amplifier. The 3-bit interpolation amplifier

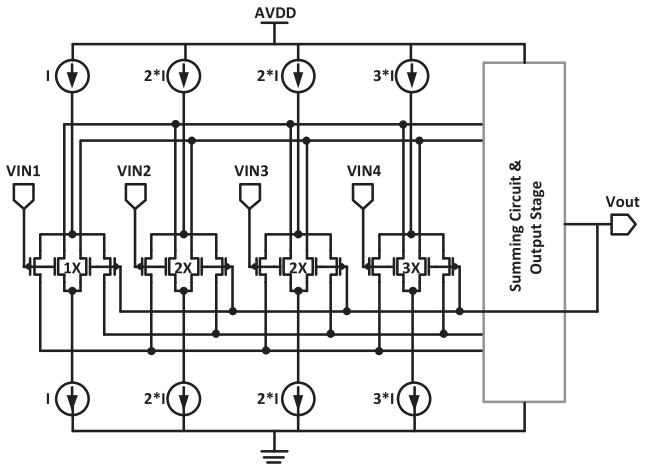

FIGURE 5 — A schematic of the proposed 3-bit interpolation amplifier.

divides into 8 voltage steps between two adjacent voltages sent from 10-bit two voltage selector. The 3-bit interpolation amplifier using input voltage modulation requires 8 input stage with same size as well input ports. These cause large input routing area. To reduce input routing area, the proposed 3-bit interpolation amplifier has 4 input stages with 1x, 2x, 2x and 3x size. Additionally, optimized layout is proposed to minimize mismatch errors.

Assuming gm is not constant with VH and VL, Vout is determined with equation 1.

$$V_{OUT} = R_O \times \sum_{i=1}^{4} g_{m,i}\left(V_{IN,i} - V_{OUT}\right) \approx \frac{\sum_{i=1}^{4}\left(g_{m,i} \times V_{IN,i}\right)}{\sum_{i=1}^{4} g_{m,i}}$$
$$V_{IN,i} = \text{VH or VL} \tag{1}$$

Difference of VH and VL is about 18mv at 18.5V of analog supply voltage. Vout is simplified with equation 2 since gm error can be negligible with 18mv difference of VH and VL.

$$V_{OUT} \approx \frac{\left(V_{IN,1} + 2\times V_{IN,2} + 2\times V_{IN,3} + 3\times V_{IN,4}\right)}{8} \tag{2}$$

when $g_{m,2} \approx g_{m,3} \approx 2 \times g_{m,1}, g_{m,4} \approx 3 \times g_{m,1}$

For example, if data input of 3-bit LSB(D2~D0) is 011, then Vout is 3/8*VH + 5/8*VL.

The proposed weighted input interpolation amplifier requires the 3-bit 2 to 4 decoder. This decoder is implemented with combination of the quaternary decoder. Table 3 shows truth table of 3-bit 2 to 4 decoder.

TABLE 3 — 2-bit Truth table for 3-bit 2 to 4 decoder.

D2	D1	D0	VIN1	VIN2	VIN3	VIN4
0	0	0	VL	VL	VL	VL
0	0	1	VH	VL	VL	VL
0	1	0	VL	VH	VL	VL
0	1	1	VH	VH	VL	VL
1	0	0	VL	VH	VH	VL
1	0	1	VH	VH	VH	VL
1	1	0	VH	VH	VL	VH
1	1	1	VL	VH	VH	VH

3 Proposed intra-panel interface

3.1 Address based configuration

Intra-panel interface protocols have a configuration field to set the function of the column driver IC, because the various functions of column driver are required in TV and IT applications.

Figure 6 (a) shows conventional 1-line data stream which has 4-fields composed of start of line (SOL), configuration, pixel data and horizontal blanking time (HBP). The detailed description of each field is as follows. SOL indicates the start point of a line data transmission. The column driver operation is set in configuration field. Pixel data stream transfers display data. HBP is allocated for charge sharing and transition of output amplifiers. The period of HBP is programmable by timing controller. In order to implement various functions with one column driver, the configuration field with different length and location is needed. However, prior works have a fixed configuration length according to each application, system overhead bits and chip size should be increased to add functions. In this paper, address based configuration protocol is proposed to minimize overhead and optimize the system.

Figure 6 (b) shows proposed addressed based configuration protocol. Packet header (PH) includes SOL packet. Proposed configuration field composed of config-length, address and configuration data. All configuration packets required in applications can be defined with address and configuration information. Therefore, the length of configuration is variable as applications and easy to expand the field. This characteristic has the advantage that can be implemented without increasing the chip size.

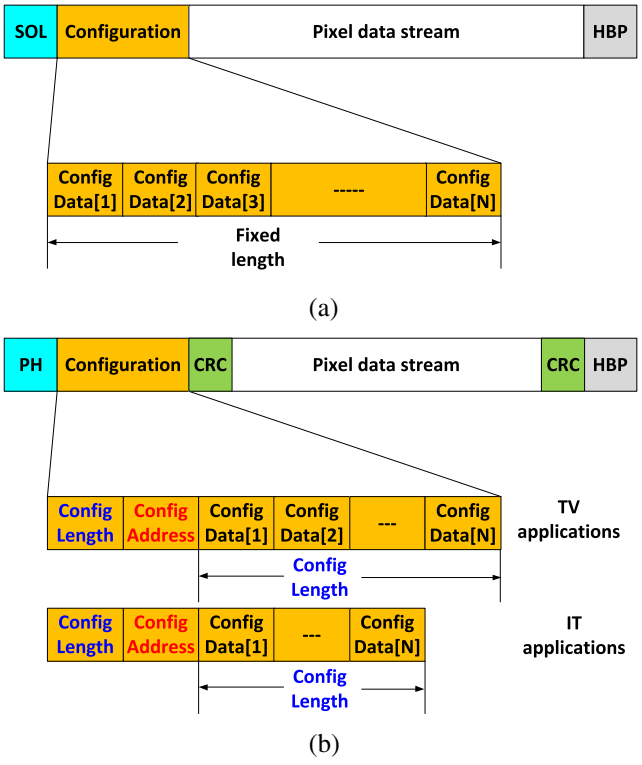

FIGURE 6 — Configuration methods in intra-panel interface. (a) conventional configuration (b) address based configuration.

3.2 High speed technique

Various display markets have continuously increased demand for high resolution and high refresh rate with high speed intra panel interfaces. Moreover, wide bandwidth interface circuits are required to use high resolution linear DAC. For example, to support UHD(7680x4320) resolution display with an proposed 13-bit DAC and 60Hz refresh rate, the data rate of intra-panel interface needs to reach up to 4.86Gbps. In order to drive up to UHD resolution with 60Hz refresh rate, an architecture of 4- ports intra-panel interface is proposed. Each port has 1.6Gbps bandwidth so that a proposed universal column driver has 6.4Gbps of total bandwidth.

When large amounts of image data are transferred with high speed data rate and multi ports, signal integrity could be poor. The proposed intra-panel interface adopted cyclic redundancy check (CRC) and error correction code(ECC) shown in Fig. 7. Two CRC detect errors in configuration field and pixel data stream, but not in Packet Header. When error occurs, receiver stops update and remains the previous configuration values and pixel data stream. ECC examines the validation of Packet Header and corrects one bit error in packet type(PT) and packet number(PN). Proposed ECC and CRC can improve signal integrity. Two kinds of configuration packet type, which are sequential access packet(SAP) and random access packet(RAP), are supported in propose intra-panel interface. The PT determines the packet type. The PN determines the length of configuration.

4 Measurement results

Table 4 shows measured performance summary of the proposed 13-bit column drivers. In large display applications

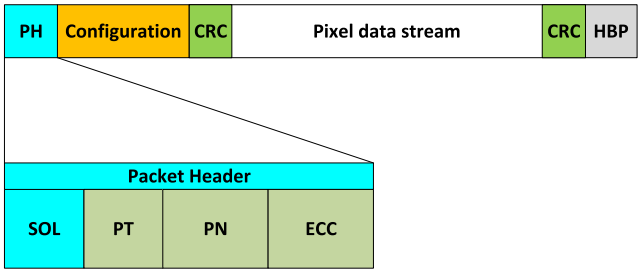

FIGURE 7 — Packet Header of the proposed intra-panel interface.

TABLE 4 — Measured performance summary of proposed column driver.

Technology	0.13-μm high-voltage CMOS process
Supply voltage	1.8V / 18.5V for column driver IC
Output range	0.2V(VREFL) to 18.3V(REFH)
Max data rate	6.4Gbps with 4 ports
Color depth	13- bit
Output channels	966
AVO (4sigma)	0.28 mV(min), 0.8 mV(max)
DVO (4sigma)	11 mV(min), 21mV(max)
INL(LSB)	−0.24(min), 2.13(max)
DNL(LSB)	−0.43(min), 0.41 (max)
Chip size	31,000 μm x 1,050 μm

using multiple column driver ICs, average voltage of outputs channels (AVO) is very critical because it can cause block dim failure. Especially AVO in mid-gray scale should be tighter than in edge-gray scale because of non linear gamma curve characteristic. Required 4-sigma value of AVO in mid-gray scale is under 2mV. Measured data shows that max 4-sigma value of AVO is 0.8mv. The value is extremely small even though 1024 resisters for R-DAC are used.

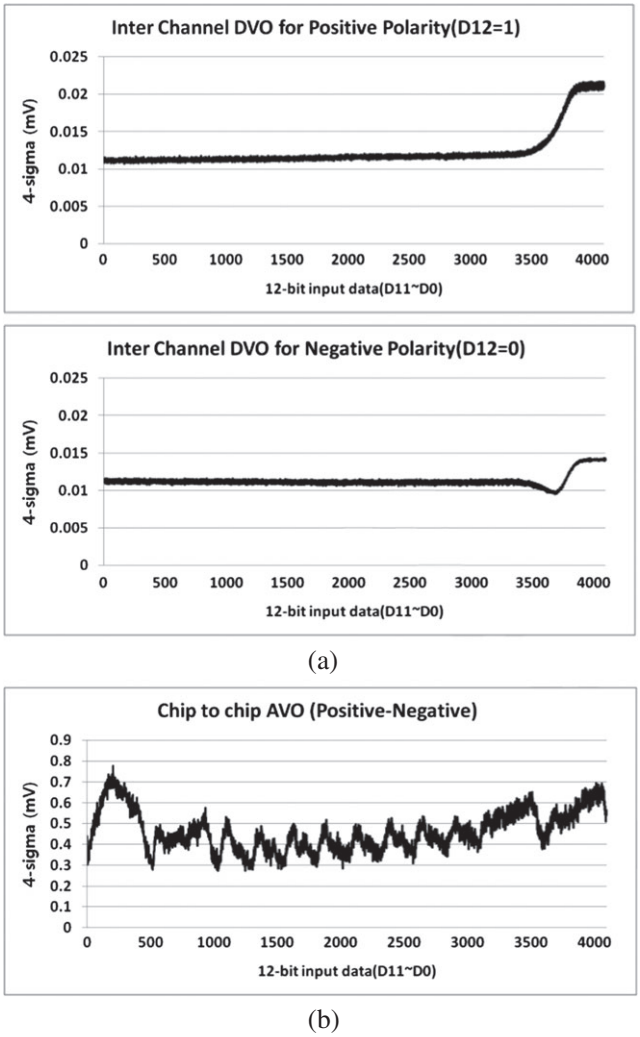

FIGURE 8 — Measurement results with proposed column driver ICs. (a) DVO (b) AVO.

Since column driver contains many channels, uniformity of different channels is important. Deviation of voltage outputs (DVO) represents uniformity of different channels. To avoid vertical line display failure, required 4-sigma value of DVO in mid-gray scale is under 20mV. Measured data shows that 4-sigma value of DVO in mid-gray is 11mv that is sufficient to meet the requirement. Figure 8 shows measured 4-sigma value of DVO and AVO.

Figure 9 (a) shows measured symmetric output voltages of the proposed 13-bit linear DAC. 13-bit input data composed of 12-bit active data(D11~D0) and 1-bit polarity control data(D12). Output voltages show monotonic performance with the 3-bit interpolation amplifier. Figure 9 (b), (c) show the measurement

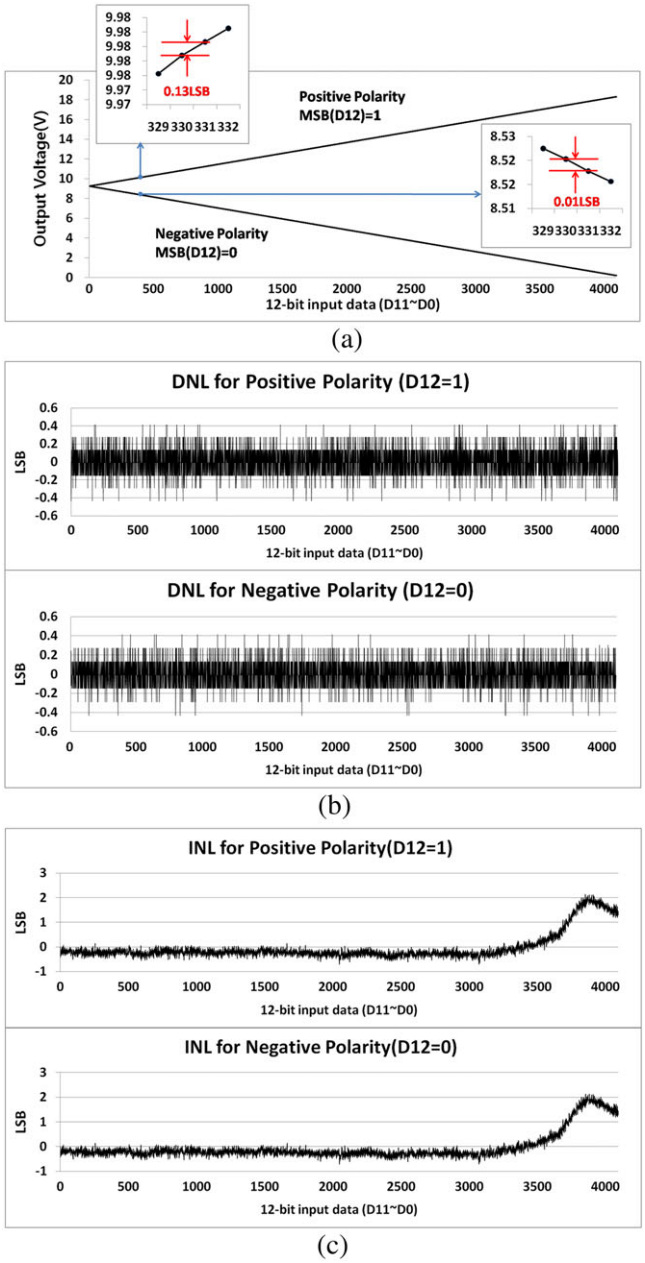

FIGURE 9 — Measurement results with one channel proposed 13-bit linear DAC. (a) Output voltage (b) DNL (c) INL.

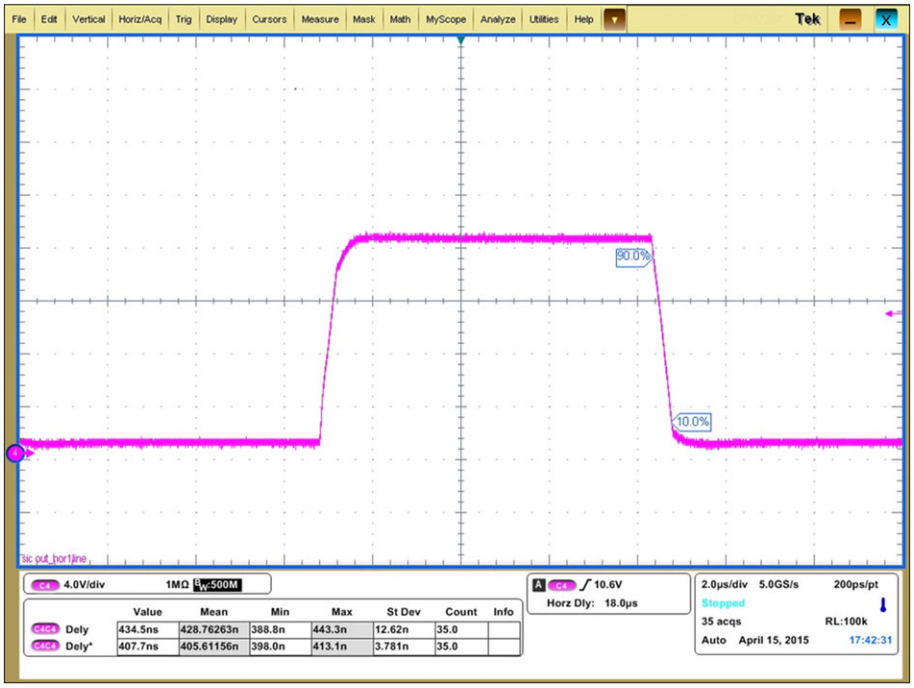

FIGURE 10 — Measured waveform of one channel output on 15.6″ TFT-LCD prototype panel for 55″ green UHD(4k).

results for performance of 13-bit linear DAC. Integral non-linearity(INL) and differential non-linearity(DNL) in mid-gray show 13-bit DAC resolution performance. INL and DNL are calculated with measured one channel output of DAC as digital input data. The reason why INL is about 2LSB around the digital code 4000 is that the one input pair of two input pairs for rail to rail operation shown in Fig. 5 turned off around digital code 4000. This causes offset increase because gm of input stage is reduced from two to one. The required resolution of the display system in edge gray is lower than in mid gray so that 2 LSB INL in edge gray could be fine. Figure 10 shows a measured waveform with 0FFFH to 1FFFH input data transition.

In this work, we could implement the system with a 15.6" TFT-LCD prototype panel for 55" green UHD(4k) as shown in Fig. 11.

FIGURE 11 — 15.6″ TFT-LCD prototype panel for 55″ green UHD(4k) with Universal Column Driver ICs.

5 Conclusion

A 13-bit universal column driver IC for various displays of OLED and LCD has been presented. This column driver is fabricated with 0.13µm process 1.8V low voltage and 18.5V high voltage devices. A chip size is 31,000 µm x 1,050 µm. The proposed 13-bit linear DAC can generate voltages corresponding to 8 to 10-bit non-linear gamma curve of LCD and OLED. The experimental results show that INL and DNL at mid gray is 0.24LSB and 0.41LSB. The proposed address based configuration in intra-panel protocol can include all column driver functions of various applications. Therefore, the proposed 13-bit universal column driver with addressed based configuration protocol can drive all applications of OLED and LCD.

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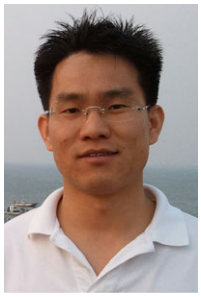

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